

TITLE 800G QSFP-DD 2XSR4 (SR8) 50m Transceiver	DOC No. RFD-20260508100-001	
	REVISION : 01	AUTHORIZED BY : Andy Yang
	DATE : 2026.05.08	CLASSIFICATION : Optical Transceiver

1. Features

- Hot-pluggable QSFP-DD form factor
- VCSEL transmitter and PIN PD receiver
- Support 850Gb/s aggregate bit rate
- Compliant with IEEE 802.3df-2024:
 - 8x100GBASE-VR1/4x200GBASE-VR2/2x400GBASE-VR/1x800GBASE-VR8 optical interface
- Compliant with IEEE 802.3df-2024:
 - 8x100GAUI-1/4x200GAUI-2/2x400GAUI-4/1x800GAUI-8 C2M electrical interface
- Compliant with QSFP-DD MSA Hardware Rev 7.0 Type 2B housing with Dual MPO-12/APC receptacle
- Compliant with CMIS Rev 5.0
- Case operating temperature 0°C to 70°C
- Power dissipation < 16W
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser

2. Production Description

3.1 Product Name and Series Numbers

800G QSFP-DD 2XSR4 (SR8) Transceiver

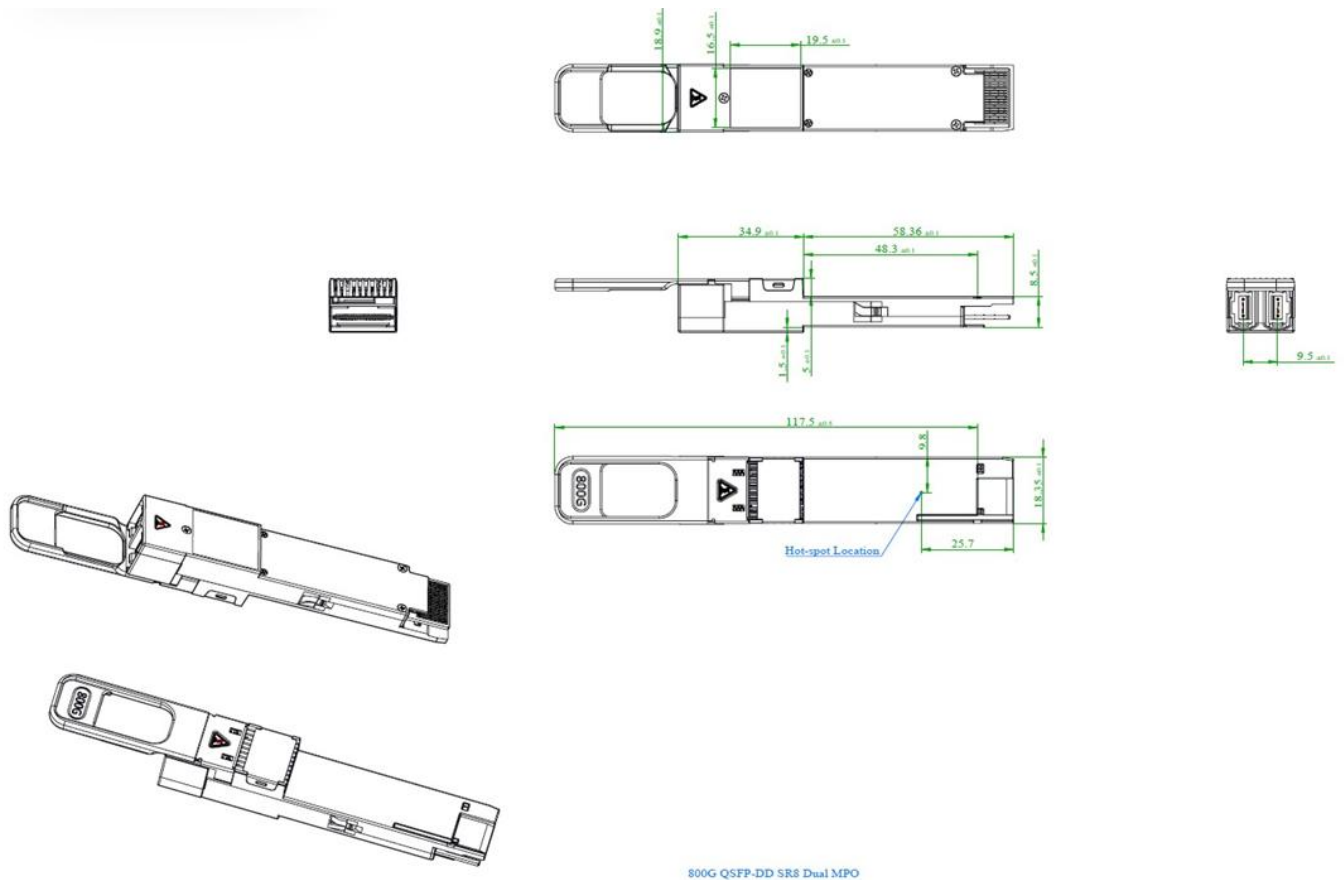
JPC P/N	Laser	Distance	Power (dBm)	Sen. (dBm)	Connector	Temp.
P66**8KRCAS5-1	850nm	50m	-4.6~4	-4.4	MPO-MMF	C

Note-1 : ** Indicates the customer code.

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3.2 Dimension, Materials, Plating and Marking

See the package outline for details.



Mechanical Package Outline (All dimensions in mm)

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3. Product Specification

3.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_s	-40	85	°C	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	85	%	
Data Input Voltage Differential	$ V_{DIP}-V_{DIN} $	-	1	V	
Control Input Voltage	V_i	-0.3	$V_{CC}+0.5$	V	
Control Output Current	I_o	-20	20	mA	

3.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Operating Case Temperature	T_{OPR}	0	-	70	°C	1
Power Supply Voltage	V_{CC}	3.135	3.3	3.46 5	V	
Instantaneous peak current at hot plug	I_{CC_IP}	-	-	640 0	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	532 8	mA	
Maximum Power Dissipation	P_D	-	-	16	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}	-	-	2	W	
Signalling Speed per Lane	DRL	-	53.125	-	GBd	

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Control Input Voltage High	V_{IH}	$V_{CC} * 0.7$	-	$V_{CC} + 0.3$	V	
Control Input Voltage Low	V_{IL}	-0.3	-	$V_{CC} * 0.3$	V	
Two Wire Serial Interface Clock Rate	-	-	-	1	MHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
Operating Distance	-	2	-	50	m	1

Note 1: 0.5 m to 30 m for OM3, 0.5 m to 50 m for OM4 and OM5, with FEC.

3.3 Transmitter Operating Characteristic-Optical

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Signaling rate, each lane (range) 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4 800GBASE-VR8 PMDs	-	53.125 ± 100 ppm 53.125 ± 50 ppm			GBd	
Wavelength	λ_c	842	-	870	nm	
RMS spectral width	RMS	-	-	0.65	dB	1
Average Launch Power, each lane	AOP_L	-4.6	-	4	dBm	
Outer Optical Modulation Amplitude (OMA _{outer}), each lane for max (TECQ, TDECQ) ≤ 1.8 dB for 1.8 < max (TECQ, TDECQ) ≤ 4.4 dB	OMA _{outer}	-2.6 -4.4+max(TECQ, TDECQ)	-	3.5	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	4.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane	TECQ	-	-	4.4	dB	
Over/under-shoot	-	-		29	%	
Transmitter power excursion, each lane	-	-		2.3	dBm	

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Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-30	dBm	
Extinction Ratio, each lane	ER	2.5	-	-	dB	
Transmitter transition time, each lane	T_r	-	-	17	ps	
RIN_{14OMA}	RIN			-132	dB/Hz	
Optical return loss tolerance	ORL			14	dB	
Encircled flux	-	$\geq 86\%$ at $19\ \mu m$ $\leq 30\%$ at $4.5\ \mu m$			-	-

3.4 Receiver Operating Characteristic-Optical

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Signaling rate, each lane (range) 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4 800GBASE-VR8 PMDs	-	$53.125 \pm 100\ \text{ppm}$ $53.125 \pm 50\ \text{ppm}$			GBd	
Wavelength	λ_{C0}	840	-	870	nm	
Damage Threshold, each Lane	AOP_D	5	-	-	dBm	
Average Receive Power, each Lane	AOP_R	-6.3	-	4	dBm	
Receive Power (OMAouter), each Lane	OMA_R	-	-	3.5	dBm	
Receiver Reflectance	RR	-	-	-15	dB	
Receiver sensitivity (OMAouter) for $TECQ \leq 1.8\ \text{dB}$ for $1.8\ \text{dB} < TECQ \leq 4.4\ \text{dB}$	S_{OMA}	-	-	- 4.4 - 6.2 + TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS	-	-	-1.8	dBm	1
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	-	4.4	-	dB	
OMAouter of each aggressor lane	-	-	3.5	-	dBm	

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Note 1: Measured with conformance test signal at TP3 for the BER = 2.4x10⁻⁴.

3.5 Electrical Specification High Speed Signal

Receiver (Module Output, TP4)						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB	-	-	-	32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode Disabled	-	-	-	600 845 35	mV	
Eye height	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	
Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Transition time	-	8.5	-	-	ps	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	
Transmitter (Module Input, TP1)						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Differential pk-pk input Voltage tolerance (TP1a)	-	750	-	-	mV	
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB	-	32 80	-	-	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5	-	-	dB	

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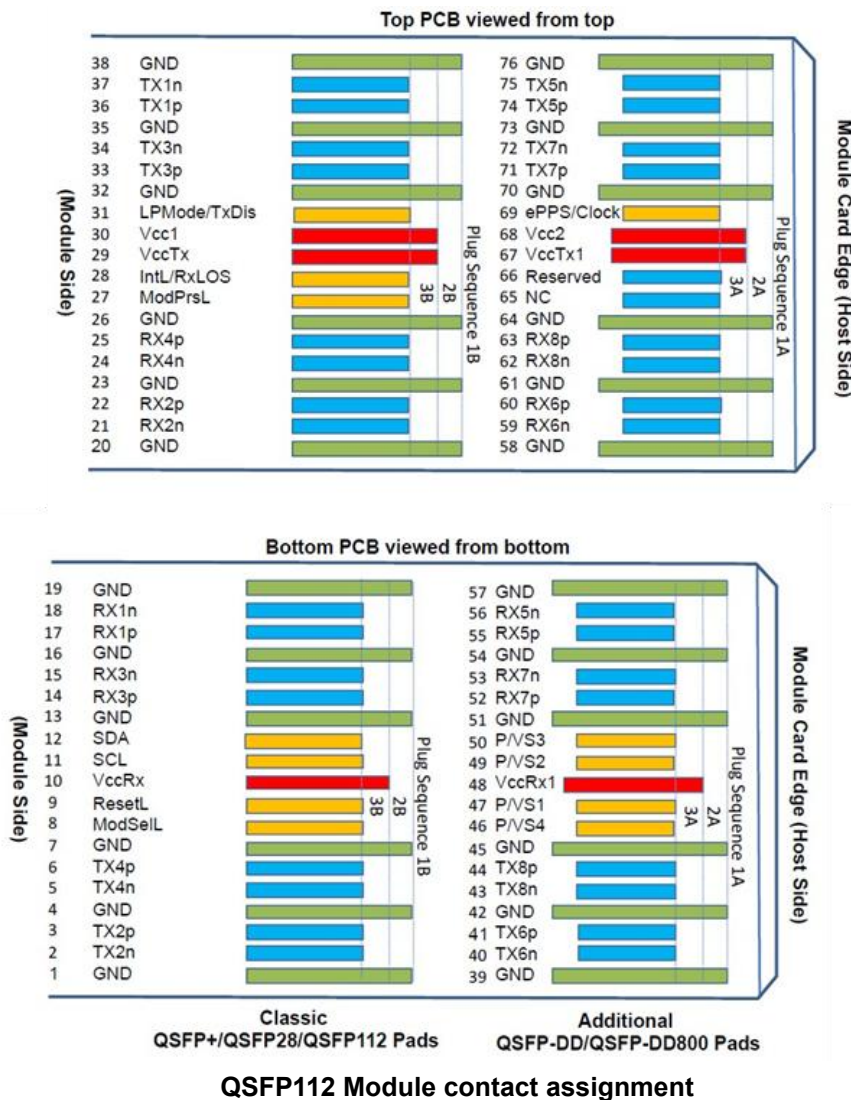
Differential termination mismatch	-	-	-	10	%	
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	

3.6 Electrical Specification Low Speed Control and Sense Signals

Parameter	Symbol	Min.	Max.	Unit	Condition
Module output SCL and SDA	V_{OL}	0	0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3	$V_{CC} \cdot 0.3$	V	
	V_{IH}	$V_{CC} \cdot 0.7$	$V_{CC} + 0.5$	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V	
	V_{IH}	2	$V_{CC} + 0.3$	V	
IntL	V_{OL}	0	0.4	V	
	V_{OH}	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V	

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4. Pin Assignments



Electrical Pin Definition

Pin #	Logic	Symbol	Definitio n	Pin #	Logic	Symbol	Definitio n
1		GND	Ground	39		GND	Ground

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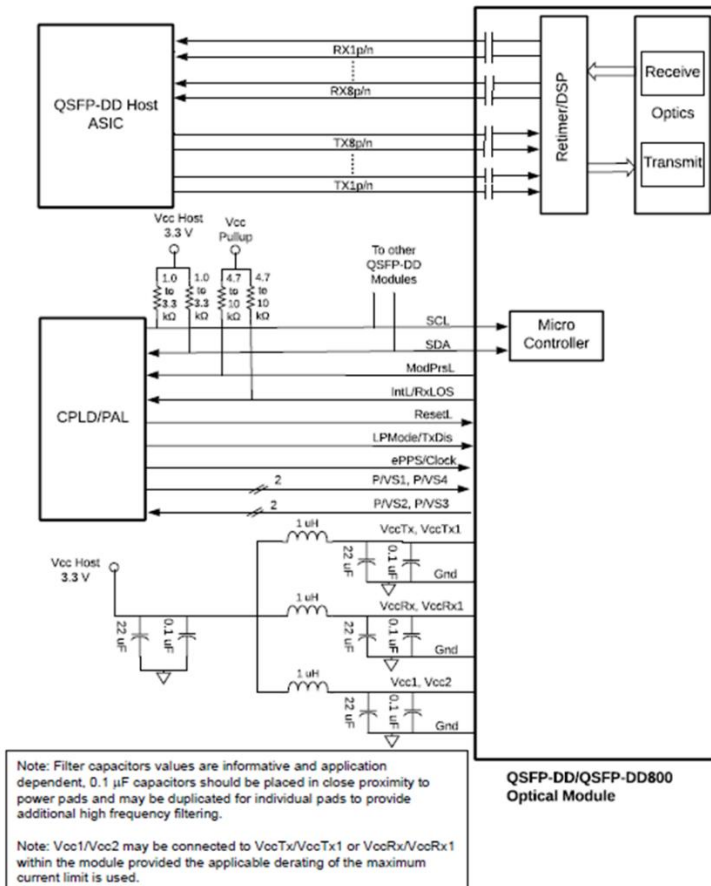
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46	LVCM O S/CML-I	P/VS4	Programmable/Module VendorSpecific 4
9	LVTTL-I	ResetL	Module Reset	47	LVCM OS /CML-I	P/VS1	Programmable/Module VendorSpecific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVC MOS -I/O	SCL	TWI serial interface clock	49	LVCM OS /CML-O	P/VS2	Programmable/Module VendorSpecific 2
12	LVC MOS -I/O	SDA	TWI serial interface data	50	LVCM OS /CML-O	P/VS3	Programmable/Module VendorSpecific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output

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23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTTL-I	LPMODE /TxDis	Low Power mode/optional TX Disable	69	LVCM OS-I	ePPS/Clock	1PPS PTP clock or reference clockinput
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

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Recommended QSFP-DD/QSFP-DD800 Host Board Schematic



Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	3.135 to 3.465	±3%	V	Internal
Tx Bias Current (Each Lane)	0 to 15	10%	mA	Internal
Tx Output Power (Each Lane)	-4.6 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-6.3 to +4	±3	dB	Internal

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5.Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2026.05.06	Andy Yang	Mike Sun